

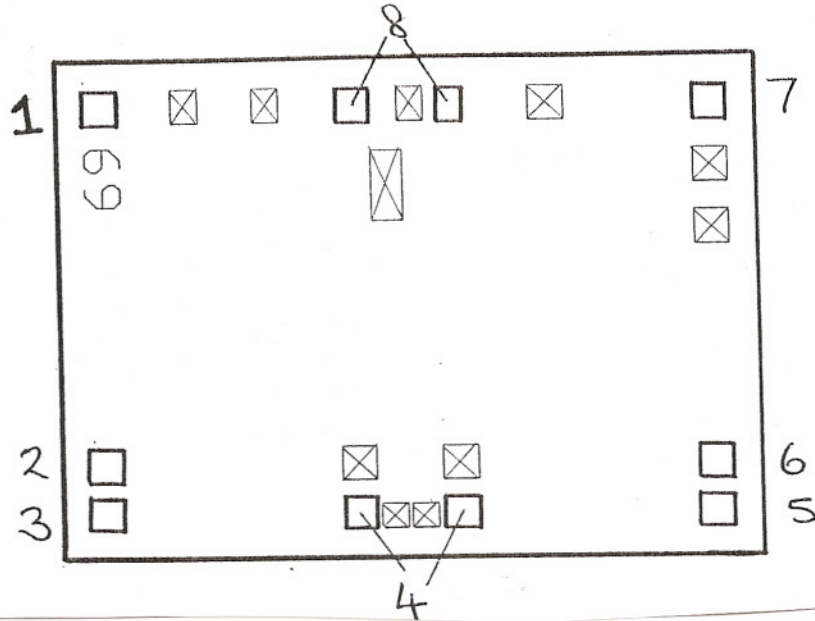


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

NOTE: The chip back may be connected to $-V_{CC}$ or left floating.



Pad	Function
1	Vout1
2	Vinv1
3	Vnon-inv1
4	$-V_{CC}$ (2 bond pads)
5	Vnon-inv2
6	Vinv2
7	Vout2
8	$+V_{CC}$ (2 bond pads)

E & O E. Dice can be supplied to this layout only if it forms part of a specification or the chip identification, if below, is requested. Chip back potential is the level at which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated above. If no potential is given the chip back should be isolated. Nominal metallisation thicknesses are based on manufacturer's information. 1 mil. = 0.001 inch. Tolerance ± 3 mils.

Topside Metal:
Backside:
Backside Potential:
Mask Ref:
Bond Pads (Mils):

APPROVED BY:
MFG: National

DIE SIZE (Mils): 78 X 78
THICKNESS:

DATE: 3/16/00
P/N: CLC428ALC

DG 10.1.2
 Rev A 3-4-99